IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Lee-Yin Chee, Kheng Guan (Nigel) Tan, Sie-Boo Chiang		
Assignee:	Advanced Micro Devices, Inc.		
Title:	Method of Generating Packets Without Repetition in Verification of a Device		
Serial No.:	10/791,914	Filing Date:	March 3, 2004
Examiner:	Kenan Cehic	Group Art Unit:	2416
Docket No.:	SE0044	Customer No.:	53362

Filed Electronically May 22, 2009

PRE-APPEAL BRIEF REQUEST FOR REVIEW AND STATEMENT OF REASONS

Sir:

Applicants request review of the January 23, 2009 Office Action. No amendments are being filed with the request. This request is being filed with a Notice of Appeal. The following sets forth a succinct, concise, and focused set of arguments for which the review is being requested.

CLAIM STATUS

Claims 2-6 are pending in the application and are rejected as obvious over U.S. Patent No. 4,862,399 to Freeman and English ADA 95: The Craft of Object-Oriented Programming, "Glossary."

REMARKS

Applicants have invented a device verification method which provides a dual-state flag for each of a plurality of packet classes so that when a packet from a packet class is generated, that packet is used to test the device for that packet class *only if* the flag for that packet class is in a first state (e.g., "0" to indicate that the packet class has not been tested), at which point the flag is changed to the second state (e.g., "1" to indicate that the packet class has been tested). *See*, claim 2. **In this way, a device is tested *by packet class* since a packet within each packet class will only be used to test the device if the flag for that packet class has not been set to the second state.** With Applicants' approach, packets need not be stored in memory, but can instead be "generated" as claimed (e.g., randomly), and each generated packet in a given packet class can be checked against the flag for that packet class to determine if the packet will be used to test the device. As explained by Applicants, the present invention eliminates the inefficient testing of devices with redundant packets (e.g., packets within the same packet class that has already been tested):

> The overall process can be described in accordance with Figure 1. Initially, each legal **packet class** is provided with a 1-bit injection flag, with each value thereof being sent (sic, set) to 0 (10). Next, a packet is randomly generated (12). The state of the injection flag of the **packet class** of the generated packet is noted (14). If the state of the injection flag is 0, the test is run (16), and the injection flag of bad (sic, that) packet class is set to 1 (18). If the state of the injection flag is 1, a test is not run, the generated packet is discarded, another packet is

> randomly generated, and the procedure subsequent thereto as described above is repeated. The process is continued until all such injection flags have been set to 1. When all the injection flags have been set to 1 (20), the simulation is ended (22).
>
> As noted, during each simulation run, only one packet **from each legal packet class** will be generated to test the controller. The problem of repetition and inefficiency described above is thus avoided, and simulation time is greatly reduced.

See, Application, page 3, line 35 to page 4, line 12 (emphasis added). Thus, instead of storing and testing redundant packets within the same packet class, Applicants have claimed using flags for each packet class to determine if a generated packet in the packet class is used to test the device.

In contrast, Freeman discloses generating and storing a small, non-redundant chip-level testset from a large, redundant chip-level testset by (1) simulating each chip-level test into its corresponding block-level tests, (2) identifying and retaining any new block-level tests in a list of "found" block-level tests, and (3) screening the chip-level tests for all block test patterns "to eliminate redundant block tests to produce a practical set of test vectors." Freeman, Abstract. The result is a non-redundant chip-level testset that is stored for subsequent use in exhaustively testing every test block on the chip. This approach is illustrated in Freeman Figure 2 and the corresponding description (col. 9, line 41 to col. 10, line 39), which shows that the large, redundant chip-level testset is stored (e.g., in the upper left storage cylinder shown in Figure 2) and then simulated "to decompose each chip-level test into its implied block-level tests for all the blocks" (as indicated in middle left block labeled "SIMULATE VIA HIGH-LEVEL MODEL" shown in Figure 2). Freeman proceeds to describe this "simulation methodology" for obtaining "fault" test patterns with reference to Figure 4. If any new block-level test patterns are found through this simulation process (as shown in the bottom left decision diamond in Figure 2), they are added to the list of previously found block-level tests (e.g., in the upper right storage cylinder shown in Figure 2). Finally, the complete list block-level tests are screened at the chip level to discard redundant chip-level test vectors that yield the same block-level test so that only one of the chip-level tests is retained as part of the "small non-redundant chip-level testset" (e.g., in the lower right storage cylinder shown in Figure 2). "This procedure is repeated for all block level tests until the test pattern P_C contains only those patterns necessary to test all blocks. This results in an efficient testset which exhaustively tests the chip in practical way for use in a factory environment." Freeman, col. 10, lines 34-39.

In rejecting claims 2-6, the Examiner asserts that the Freeman disclosure (Figs. 2 and 4 and col. 9, line 40 to col. 10, line 40) meets the claim requirements except for the various recitations of a dual state "flag" and changes thereto, which the Examiner asserts is met by the disclosure from English at page 5 (definition of "Flag"). *See*, Office Action, pp. 2-12. In response, Applicants submit that neither Freeman nor English disclose or suggest "providing a plurality of packet classes," much

less "providing a flag ... for each of the plurality of packet classes" as recited in each of the pending claims. On this point, Applicants have carefully review the cited "test pattern" disclosure from Freeman, but there is absolutely no teaching or suggestion by Freeman of any "packet class" test pattern, much less of providing any "indication" (or flag) for each "packet class." Even if one (improperly) assumes that English's "flag" would be combined with Freeman's system, there is simply no teaching or suggestion that Freeman's test pattern simulation methodology provides "a plurality of packet classes," much less that any of English's flags would be provided "for each of the plurality of packet classes," as recited in the claims. Instead of being concerned with testing by packet class, Freeman is concerned with generating a chip-level test pattern P_C which "contains only those patterns necessary to test all blocks." Freeman, col. 10, lines 34-39. As for the Examiner's Advisory Action argument that English's "flag" would be used to "note" the "detected" patterns as shown in Figure 4, Applicants submit that there is no flag-based device test decision disclosed or suggested, such as the requirement in claims 2-3 and 5 of testing the device "if the flag of the packet class of the generated packet is in the first state," or the requirement in claims 3-5 of not testing the device "if the flag of the packet class of the generated packet is in the second state." Based on at least these deficiencies, Applicants submit that a *prima facie* obviousness case has not been established. *See*, MPEP, § 2143.03 ("All words in a claim must be considered in judging the patentability of that claim against the prior art"). When determining whether a claim is obvious, an Examiner must make "a searching comparison of the claimed invention - *including all its limitations* - with the teaching of the prior art." In re Ochiai, 71 F.3d 1565, 1572 (Fed. Cir. 1995) (emphasis added). Since there is no disclosure by the asserted combination of Freeman and English of testing a device *by packet class* by using a packet within each packet class to test the device only if the flag for that packet class has not been set to the second state, the claimed invention is not obvious.

In addition to the missing claim requirements, Applicants submit that a person having ordinary skill in the art would not have combined the Freeman and English references in the first place. On this point, the Examiner asserts that:

> It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Freeman by using the features, as taught by English, in order to provide an means/programming technique (using flags) which indicates a certain state of a program/variables with minimal storage (memory) use.... Furthermore, each of the claimed elements was known in the art, and a person of ordinary skill in the art could have combine the use of flags into the program/method of Freeman each element would have preformed the same function as it did separately. The use of flags in the Freeman system would not change the operation of the Freeman system, as the use of flags is merely using variables in a program that indicate a certain state and one of ordinary skill in the art would have recognized that the results of the combination would have been predictable.

Office Action, pp. 12-13 (emphasis added). While this quote is not entirely clear about what "program/variables" from Freeman are being indicated "using flags," the Examiner appears to be arguing that the detected block-level "fault" testsets shown in Figure 4 "could" have been indicated using English's flags. But the proper legal standard is not what could a person having ordinary skill in the art do. Instead, the question is what would such a person do. And in this case, the Examiner has failed to show how a person skilled in the art would be motivated to combine the references. *See*, DyStar Textilfarben GMBH v. C. H. Patrick Co., 464 F.3d 1356, 80 USPQ2d 1641 (Fed. Cir. 2006) ("'[C]onclusory statements such as those here provided do not fulfill the agency's obligation' to explain all material facts relating to a motivation to combine."). As required by the recent KSR decision, the Examiner must provide "some articulated reasoning with some rationale underpinning to support the legal conclusion of obviousness" and must "identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." KSR v. Teleflex, 127 S. Ct. 1727, 82 U.S.P.Q.2d 1385 (2007). In addition, the Examiner must make "explicit" this rationale of "the apparent reason to combine the known elements in the fashion claimed," including a detailed explanation of "the effects of demands known to the design community or present in the marketplace" and "the background knowledge possessed by a person having ordinary skill in the art." Id. Anything less than such an explicit analysis does not meet the requirement of a *prima facie* case of obviousness.

Applicants respectfully submit that inclusion of a flag with Freeman's system as suggested by the Examiner is not indicative of "minimal storage use" and "minimal memory and processing resources" as compared to Freeman itself. Instead of storing flag information for every possible block-level and chip-level testset, Freeman's approach (described at column 10 at lines 26-39) is to "discard" redundant block-level and chip-level tests, resulting in smaller memory storage requirements and reduced processing requirements since only the required tests are stored and processed. To add a flag storage requirement as proposed by the Examiner would actually increase the requirements for storing and processing the flag information, especially if all of the block-level and chip-level tests are being stored with the additinal flag information.

In *direct* contradiction to the Examiner's assertion that it would be obvious to combine English's flag with Freeman's testset generation system, Applicants would note that Freeman's approach -- for identifying and storing block-level tests from each chip-level test simulation, along with the non-redundant chip-level tests -- would not be combined with English's disclosure – of

using flags "to indicate a certain property/state of either the program/variable" -- since these references conflict with one another. If the Examiner is proposing to replace Freeman's detected and stored testsets with "the use of flags," this combination would render the Freeman reference wholly unsatisfactory for its intended purpose since the whole objective from Freeman is to generate an efficient, non-redundant set of chip-level and block-level tests. Simply storing "known flags to indicate a certain property/state of either the program/variable" as suggested by the Examiner simply won't get the job done. *See*, MPEP § 2143.01(V) ("If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)."). Alternatively, if the Examiner is proposing to supplement and modify Freeman's system for detecting and storing testsets by including program/variable flags along with all chip-level and block-level tests, this combination would change the principle of operation of the Freeman system which uses an *additive* process to *selectively* identify and store only non-redundant chip-level tests and "new" block-level tests (along with "already found" block-level tests). *See*, MPEP § 2143.01(VI) ("If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious.") (citing In re Ratti, 123 USPQ 349 (CCPA 1959)). In the absence of a *prima facie* showing that the requirements of claims 2-6 are disclosed in or obvious over the prior art, or that the Freeman and English references would be combined in the first place, Applicants request that the obviousness rejection of claims 2-6 be withdrawn and that the claims be allowed.

CONCLUSION

In view of the remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at 512-338-9100.

CERTIFICATE OF TRANSMISSION

I hereby certify that on May 22, 2009, this correspondence is being transmitted via the U.S. Patent & Trademark Office's electronic filing system.

/Michael Rocco Cannatti/

Respectfully submitted,

/Michael Rocco Cannatti/

Michael Rocco Cannatti
Attorney for Applicant(s)
Reg. No. 34,791